

FIG. 1
programmable logic device 10

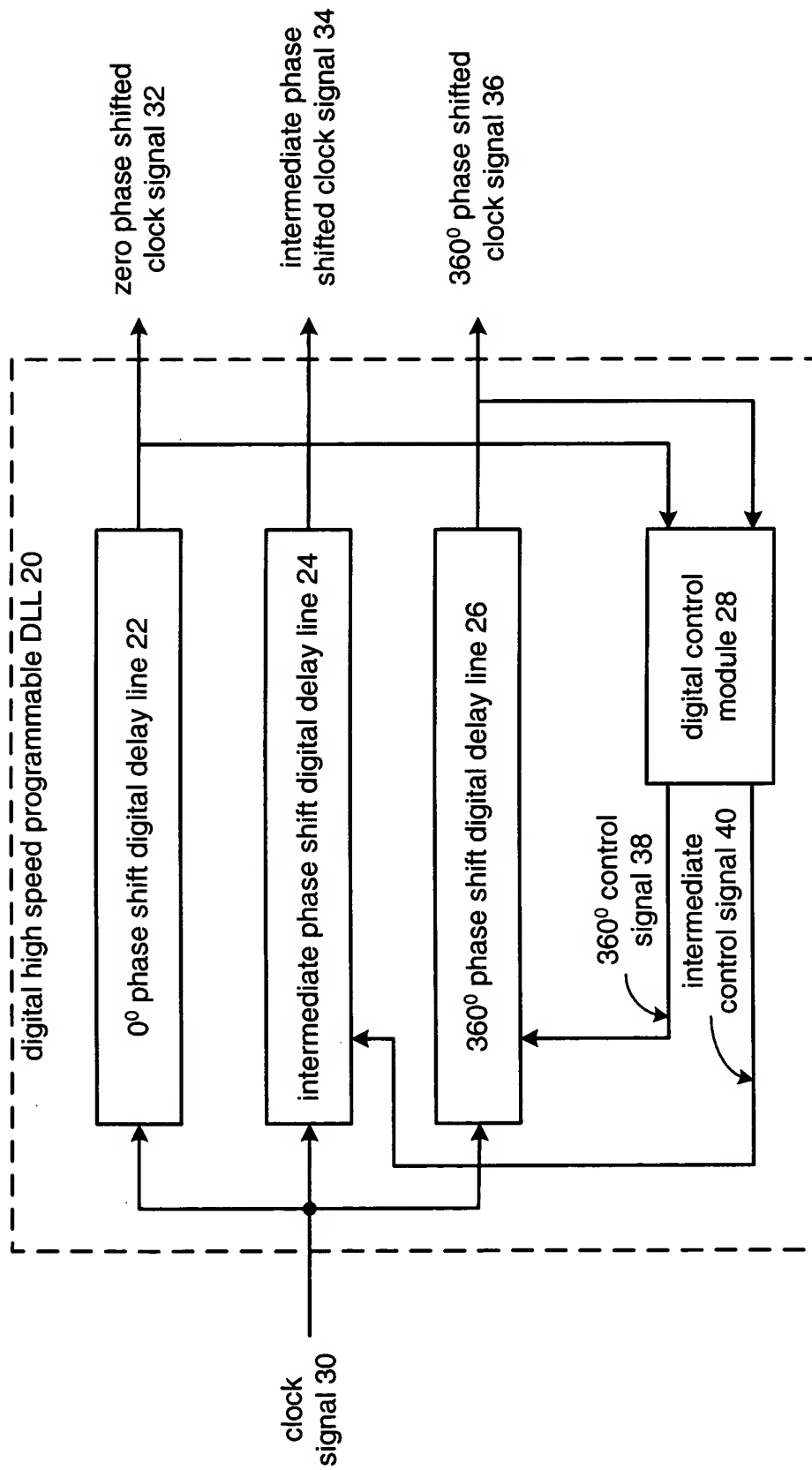


FIG. 2
digital clock manager

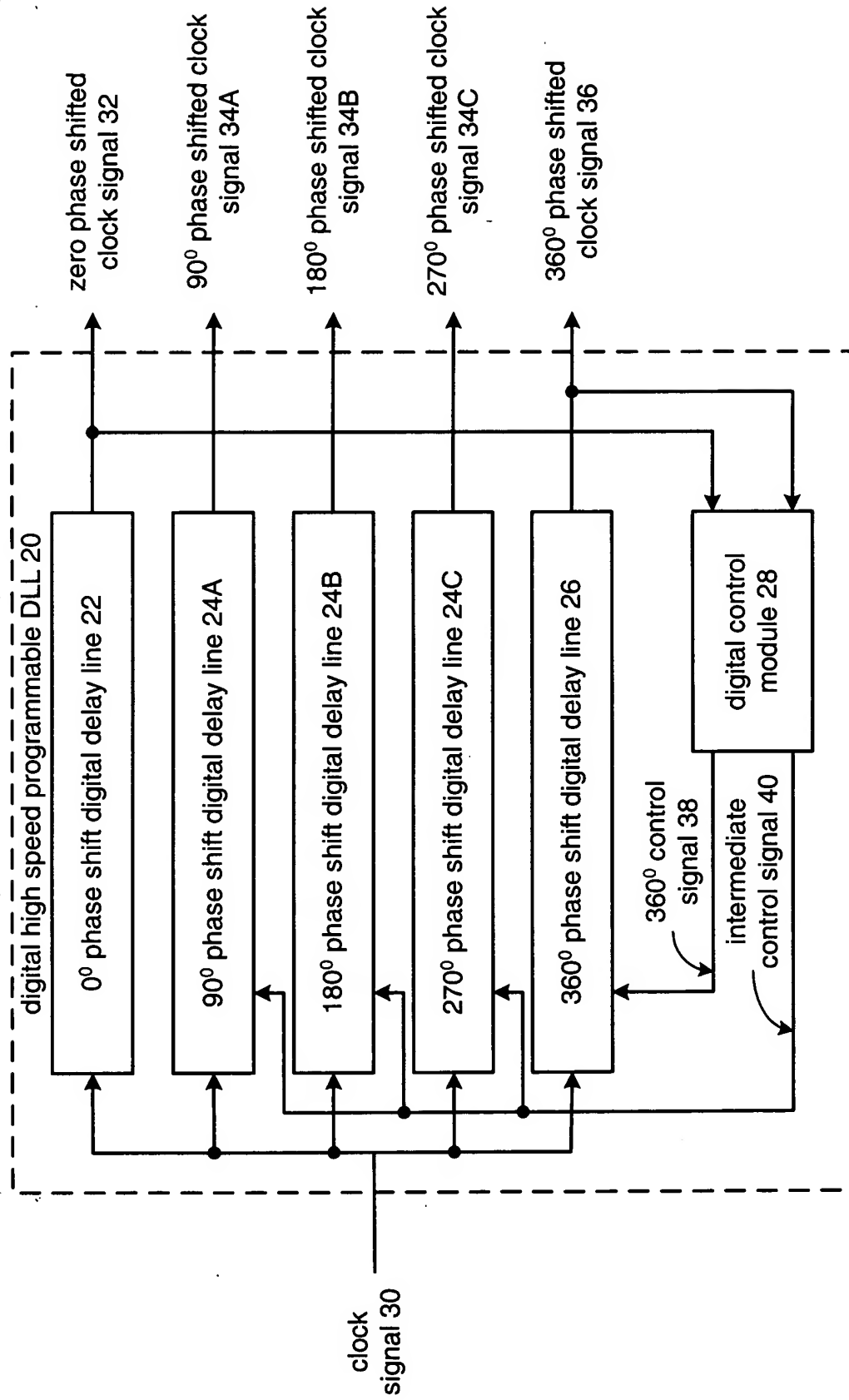


FIG. 3

digital clock manager

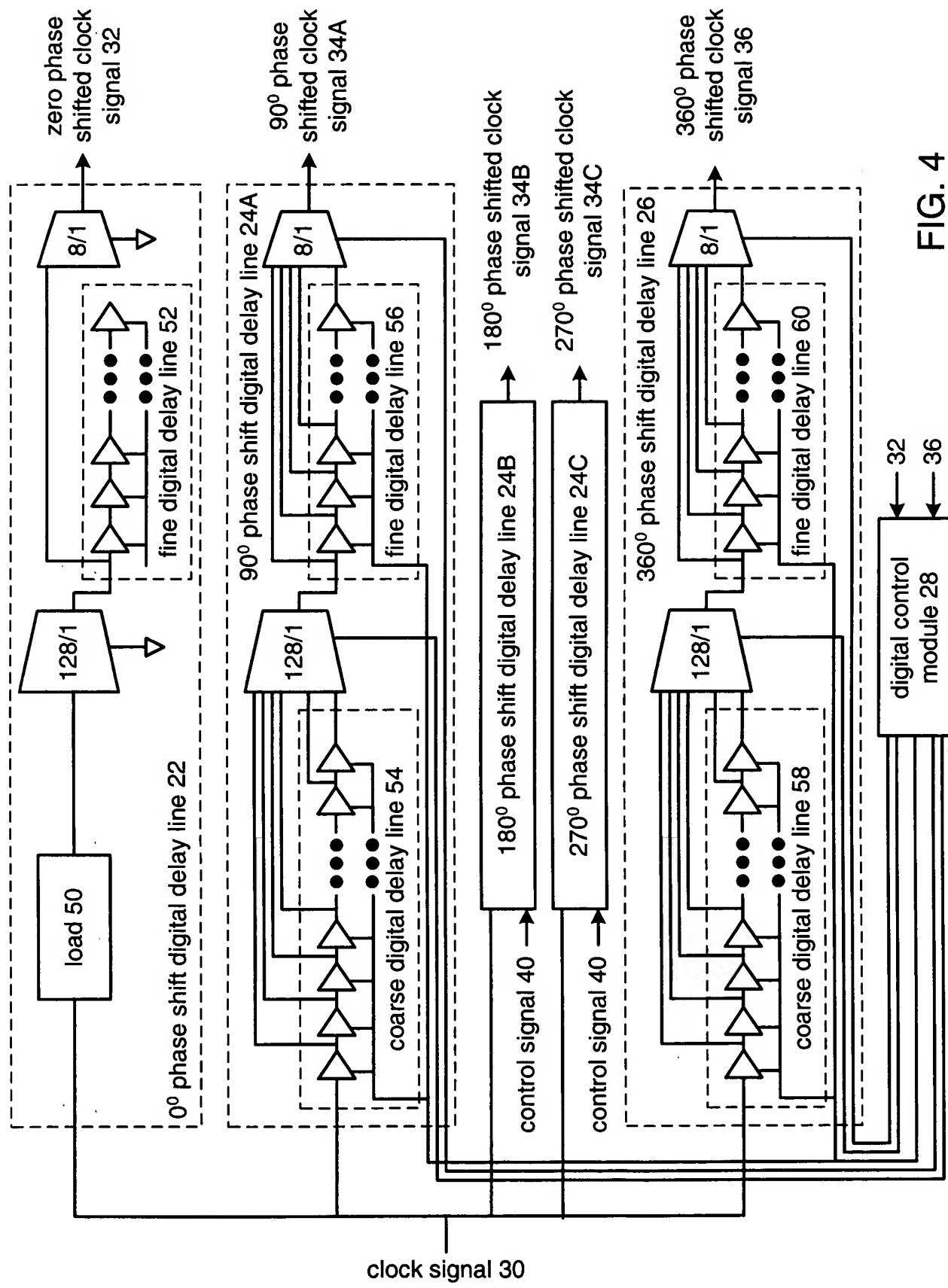


FIG. 4

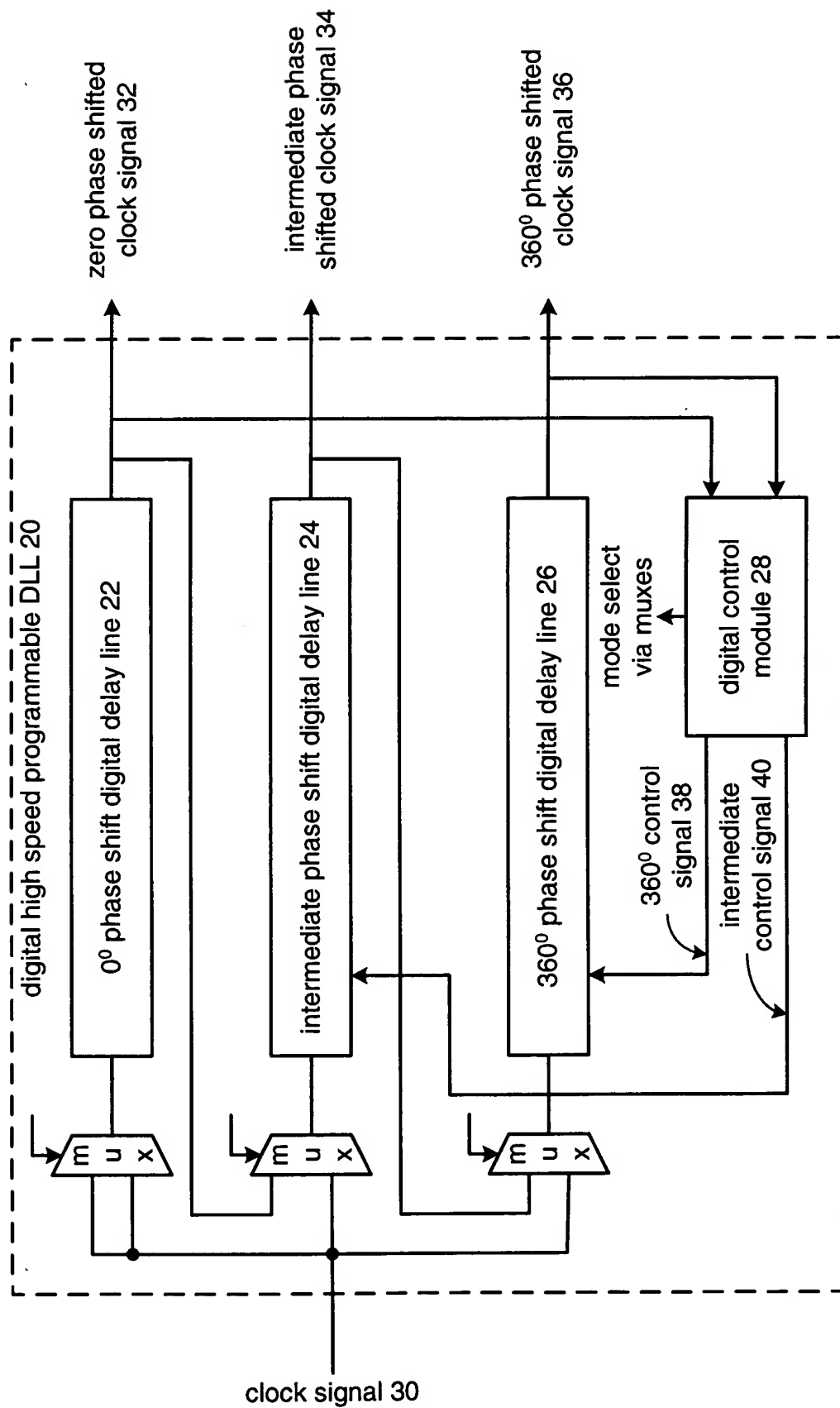


FIG. 5

digital clock manager